



BLUE CHIP TECHNOLOGIES

Joining the Poles apart

TECHNOLOGY : VLSI

DOMAIN : IEEE TRANSACTIONS ON IMAGE PROCESSING

SL.NO	CODE	PROJECT TITLE	YEAR
1	IPEVLO1	A PROCESSOR IN MEMORY ARCHITECTURE FOR MULTIMEDIA COMPRESSION	2007
2.	IPEVLO2	A VLSI PROGRESSIVE CODING FOR WAVELET BASED IMAGE COMPRESSION	2007
3.	IPEVLO3	REDUCED COMPLEXITY DELAYED ALGORITHM FOR CONTEXT BASED IMAGE PROCESSING SYSTEM	2007
4.	IPEVLO4	A MEMORY EFFICIENT PROGRESSIVE JPEG DECODER	2007
5.	IPEVLO5	A METHOD TO PERFORM A FFT WITH PRIMITIVE IMAGE TRANSFORMATIONS	2007

TECHNOLOGY : VLSI

DOMAIN : : IEEE TRANSACTIONS ON COMMUNICATIONS

SL.NO	CODE	PROJECT TITLE	YEAR
1	ICEVLO1	HIGH SPEED RECURSION ARCHITECTURE FOR MAP- BASED TURBO DECODERS	2007
2.	ICEVLO2	REGISTER FOR PHASE DIFFERENCE BASED LOGIC	2007
3	ICEVLO3	SHIFT REGISTER BASED DATA TRANSPOSITION FOR COSE EFFECTIVE DISCRETE COSINE	2007

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Coimbatore: 9962 065 075, **Erode:** 9962 064 074, **Trichy:** 9962 063 073,

Salem: 9962 067 077, **Madurai:** 9962 060 070, **Tirunelveli:** 9962 061 071

		TRANSFORM	
4	ICEVLO4	A ROBUST UART ARCHITECTURE BASED ON RECURSIVE RUNNING SUM FILTER FOR BETTER NOISE PERFORMANCE.	2007
5	ICEVLO5	DIGITAL DESIGN OF DS-CDMA TRANSMITTER USING VHDL AND FPGA	2006

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 DOMAIN :IEEE TRANSACTIONS ON VLSI

SL.NO	CODE	PROJECT TITLE	YEAR
1	IVLSIC01	FPGA IMPLEMENTATION OF LOW POWER PARALLEL MULTIPLIER	2007
2.	IVLSIC02	DESIGNING EFFICIENT ONLINE TESTABLE REVERSIBLE ADDER WITH NEW REVERSABLE GATE	2007
3	IVLSIC03	COMPACT HARDWAE DESIGN OF WHIRLPOOL HASHING CORE	2007
4	IVLSIC04	IMPLEMENTATION OF AES ON A DYNAMICALLY RECONFIGURABLE ARCHITECTURE.	2007
5.	IVLSIC05	CONCURRENT ERROR DETECTION IN REED SOLOMON ENCODERS AND DECODERS	2007
6	IVLSIC06	ABSTRACTION AND REFINEMENT TECHNIQUES IN AUTOMATED DESIGN DEBUGGING	2007
7.	IVLSIC07	NOVEL BCD ADDERS AND THEIR REVERSIBLE LOGIC IMPLEMENTATION FOR IEEE 754R FORMAT.	2006
8.	IVLSIC08	SHIFT INVERT CODING FOR LOW POWER VLSI	2004
9.	IVLSIC09	REAL TIME ADAPTIVE SPEECH WATERMARKING SCHEME FOR MOBILE APPLICATIONS	2003
10.	IVLSIC10	A LIGHTWEIGHT ENCRYPTION METHOD SUITABLE FOR COPYRIGHT PROTECTION	1998

TECHNOLOGY: VLSI USING VHDL/VERILOG
 DOMAIN: COMMUNICATION

S.NO	CODE	PROJECT TITLE
1.	VLSIO1	RTL DESIGN AND SIMULATION OF MICRO CONTROLLER IN HDL
2.	VLSIO2	RTL DESIGN AND SIMULATION OF 8 - BIT

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		CPU IN HDL
3.	VLSI03	DESIGN AND IMPLEMENTATION OF FLOATING POINT ADDER UNIT IN VHDL
4.	VLSI04	RTL DESIGN AND COMPARISON FOR VARIOUS MULTIPLIER ARCHITECTURES
5.	VLSI05	HDL IMPLEMENTATION OF ERROR DETECTION AND CORRECTION CIRCUIT
6.	VLSI06	DESIGN AND IMPLEMENTATION OF HIGH SPEED MATRIX MULTIPLIER BASED ON WORD-WIDTH DECOMPOSITION
7.	VLSI07	RTL SIMULATION OF QPSK MODEM
8.	VLSI08	DESIGN AND IMPLEMENTATION OF 64 POINT FFT / IFFT FOR IEEE 802.11A
9.	VLSI09	DESIGN AND IMPLEMENTATION OF DIRECT DIGITAL SYNTHESIZERS FOR WIRELESS APPLICATIONS
10.	VLSI10	DESIGN AND IMPLEMENTATION OF DIGITAL DOWN CONVERTER (DDC) =M.E
11.	VLSI11	DESIGN AND IMPLEMENTATION OF DIGITAL UP CONVERTER (DUC) =M.E
12.	VLSI12	DESIGN AND IMPLEMENTATION OF SECOND ORDER COSTOS LOOP FOR BPSK MODEM
13.	VLSI13	DESIGN AND IMPLEMENTATION OF SECOND ORDER COSTOS LOOP FOR QPSK MODEM
14.	VLSI14	HDL IMPLEMENTATION OF LOGARITHMIC AND ANTILOGARITHMIC CONVERTER
15.	VLSI15	DESIGN AND IMPLEMENTATION OF LMS ALGORITHM IN VHDL
16.	VLSI16	IMPLEMENTATION OF DCT/IDCT ALGORITHM IN VHDL
17.	VLSI17	IMPLEMENTATION OF WAVELET BASED COMPRESSION ALGORITHM IN HDL
18.	VLSI18	DESIGN AND IMPLEMENTATION OF VLIW STACK PROCESSOR IN HDL
19.	VLSI19	DESIGN AND IMPLEMENTATION OF ALU IN HDL
20.	VLSI20	DESIGN AND IMPLEMENTATION OF DDFS IN HDL
21.	VLSI21	RTL SIMULATION OF VITERBI ALGORITHM
22.	VLSI22	DESIGN AND IMPLEMENTATION OF REED SOLOMON ENCODER IN HDL

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